Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-25   (canceled)

Claim 26 (currently amended):   A method comprising:

transferring pixel data to a transformation engine at a given memory address range;

performing a transformation on the pixel data; and

readdressing the transformed pixel data to another memory address range using the transformation engine and without using a fetch engine.

Claim 27 (previously presented):   The method of claim 26 further including:

manipulating the transformed pixel data without going between a memory location and another transformation engine.

Claim 28 (previously presented):   The method of claim 27 further including:

writing pixel data to a first virtual memory location; and

performing a first pixel transformation at said first virtual memory location in a virtual memory space.

Claim 29 (previously presented):   The method of claim 28 further including:

generating a virtual memory address for a second memory location.

Claim 30 (currently amended):   The method of claim 29 further inleuding including:

re-mapping a virtual memory address of said first virtual memory location to write said transformed pixel data from said first virtual memory location to said virtual memory address of said second memory location; and

transferring the pixel data to a memory controller using a memory controller client in a forward, write-through direction.

Claim 31 (previously presented):   The method of claim 30 further including writing pixel data to a virtual memory location associated with a memory controller client that receives pixel data written to certain virtual addresses.

Claim 32 (previously presented):   The method of claim 31 including causing an operating system to set aside virtual addresses for said memory controller client.

Claim 33 (previously presented):   The method of claim 30 wherein generating said virtual memory address for said second memory location includes transforming the addresses of said pixel data at said first virtual memory location to addresses at said second memory location.

Claim 34 (previously presented):   The method of claim 33 including determining the offset to pixel data by subtracting a base address at said first virtual memory location from the address of pixel data.

Claim 35 (previously presented):   The method of claim 34 including adding said offset to a base address of said second memory location.

Claim 36 (currently amended):   The method of claim 30 wherein writing said transformed pixel data from said first virtual memory location to said second memory location includes writing the pixel data from said first virtual memory location associated with a first transfer function that performs the transformation on the pixel data to said second memory location associated with a second transfer function that performs a second transformation on the transformed pixel data.

Claim 37 (previously presented):   The method of claim 36 including transforming the addresses of the pixel data from addresses in a first virtual memory range associated with said first transfer function to memory addresses in a second virtual memory range associated with said second transfer function.

Claim 38 (currently amended):   An article comprising a medium storing instructions that enable a processor-based system to:

transfer pixel data to a transformation engine at a given memory address range;

perform a transformation on the pixel data; and

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readdress the transformed pixel data to another memory address range <u>using the transformation engine and</u> without using a fetch engine.

Claim 39 (previously presented):   The article of claim 38 further storing instructions that enable the processor-based system to:

manipulate the transformed pixel data without going between a memory location and another transformation engine.

Claim 40 (previously presented):   The article of claim 39 further storing instructions that enable the processor-based system to:

write pixel data to a first virtual memory location; and

perform a first pixel transformation at said first virtual memory location in a virtual memory space.

Claim 41 (previously presented):   The article of claim 40 further storing instructions that enable the processor-based system to:

generate a virtual memory address for a second memory location.

Claim 42 (previously presented):   The article of claim 41 further storing instructions that enable the processor-based system to:

re-map a virtual memory address of said first virtual memory location to write said transformed pixel data from said first virtual memory location to said virtual memory address of said second memory location; and

transfer the pixel data to a memory controller using a memory controller client in a forward write-through direction.

Claim 43 (previously presented):   The article of claim 42 further storing instructions that enable the processor-based system to write pixel data to a virtual memory location associated with a memory controller client that receives pixel data written to certain virtual addresses.

Claim 44 (previously presented):   The article of claim 43 further storing instructions that enable the processor-based system to cause an operating system to set aside virtual addresses for said memory controller client.

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Claim 45 (previously presented):   The article of claim 42 further storing instructions that enable the processor-based system to transform the addresses of pixel data at said first virtual memory location to addresses at said second memory location.

Claim 46 (previously presented):   The article of claim 45 further storing instructions that enable the processor-based system to determine the offset to each pixel data by subtracting a base address at said first virtual memory location from the address of each pixel data.

Claim 47 (previously presented):   The article of claim 46 further storing instructions that enable the processor-based system to add said offset to a base address of said second memory location.

Claim 48 (currently amended):   The article of claim 42 further storing instructions that enable the processor-based system to write said pixel data from said first virtual memory location associated with a first transfer function that performs the transformation on the pixel data to said second memory location associated with a second transfer function that performs a second transformation on the transformed pixel data.

Claim 49 (previously presented):   The article of claim 48 further storing instructions that enable the processor-based system to transform the addresses of said pixel data from addresses in a first virtual memory range associated with said first transfer function to memory addresses in a second virtual memory range associated with said second transfer function.

Claim 50 (currently amended):   A system comprising:

a memory controller that receives to receive pixel data and virtual memory addresses for a transformation of the pixel data in a virtual memory space;

a first memory controller client that forwards to forward the pixel data and virtual memory addresses to a first transfer function to perform the transformation of the pixel data; and

a second memory controller client that receives to receive data from said first transfer function together with new virtual memory addresses for transfer in a forward, write-through direction without using a fetch engine.

Claim 51 (currently amended):   The system of claim 50 wherein said first memory controller client is to selectively forwards forward the pixel data and virtual memory addresses to one of a plurality of transfer functions and said second memory controller client receives is to

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receive the pixel data with new virtual memory addresses from the one of said plurality of transfer functions.

Claim 52 (currently amended): The system of claim 51 wherein said second memory controller client writes is to write the pixel data back to said memory controller.

Claim 53 (currently amended): The system of claim 50 including a plurality of transfer functions to perform transformations on the pixel data, one of said transfer functions arranged to write output data to an address range of another of said transfer function functions.

Claim 54 (previously presented): The system of claim 53 wherein said transfer functions are associated with virtual memory address ranges.